In the Claims

1. (Currently Amended) A single-die integrated circuit for switching among a plurality of transmission ports and a plurality of received reports, comprising:

a transmitter switching section having a plurality of transmission ports, said transmitter ~~control circuitry~~ switching section operable to switch a selected one of the plurality of transmission ports to a transmission node wherein, for each transmission port, the transmission switching section includes a plurality of FETs having current paths coupled in series with each other and operable to couple the transmission port to the transmission node, wherein a first one of the FETs proximate the respective transmission port has a current path with a first end coupled to the transmission port and a gate;

a first feed-forward capacitor coupled between said first end of said current path and said gate of said first one of the FETs; and

a receiver switching section having a plurality of received ports, said receiver ~~control circuitry~~ switching section operable to switch a selected one of the plurality of received reports to the transmission node.

2. (Original) The integrated circuit of Claim 1, wherein the receiver switching section includes at least two cascaded stages, a first cascaded stage controllable to switch the transmission node to a receiver node, a second cascaded stage controllable to switch the receiver node to a selected one of the plurality of receiver ports.

3. (Original) The integrated circuit of Claim 1, and further comprising an antenna port coupled to the transmission node.

4-8. (Cancelled)

9. (Currently Amended) The integrated circuit of Claim ~~4~~ 1, wherein at least one of the FET switching topologies includes at least one FET having a plurality of contiguous source regions interdigitated with a plurality of contiguous drain regions, a sinuous gate formed to wind between the source regions and the drain regions.

10. (Currently Amended) A single-die multiband switch for wireless communication, comprising:

an antenna port;

a plurality of transmitter ports, for each transmitter port a switching topology operable to switch the ~~last said~~ transmitter port to the antenna port; and

a plurality of received ports, ~~for each receiver port~~

a switching topology operable to switch ~~the last~~ a selected one of said receiver ~~port~~ ports to the antenna port, said switching topologies comprising a multiple-stage switching circuit, a first stage of the multiple-stage switching circuit selectively connecting or isolating the antenna port from the multiple-stage

switching topology, and a last stage of the multiple-stage switching topology selectively connecting or isolating a plurality of the receiver ports from the multi-stage switching topology, wherein said last stage includes, for each receiver port, a signal path FET having a current path controllable to connect the receiver port to an intermediate node, said first stage operable to connect the intermediate node to the antenna port, and wherein each said signal path FET has a gate to which a control signal is applied, a shunt FET having a drain coupled to the gate of the signal path FET, a source coupled to ground, and operable to enhance isolation of the receiver port from the intermediate node when the signal path FET is in and OFF state.

11. (Currently Amended) The switch of Claim ~~7~~ 10, wherein ~~at least one of the~~ said first stage of said switching topology ~~topologies~~ comprises a plurality of series-connected field effect transistors, wherein a control signal for said ~~at least one~~ switching topology ~~controlling~~ controls said ~~at least one~~ switching topology to selectively connect or isolate a respective transmitter or receiver port from the antenna port.

12. (Currently Amended) The switch of Claim ~~7~~ 10, wherein at least one of the switching topologies comprises at least one interdigitated field effect transistor having a plurality of elongated contiguous drain regions, a plurality of elongated contiguous source regions interdigitated with the drain regions, an

elongated sinuous channel region spacing apart the drain regions from the source regions, and a gate overlying the channel region to switch the interdigitated field effect transistor between an ON and an OFF state.

13. (Currently Amended) The switch of Claim ~~7~~ 10, wherein the die has an area, the transmitter port switching topologies occupying an area on the die which is substantially larger than the receiver port switching topologies..

14-20. (Cancelled).

21. (Currently Amended) A method of switching one of a plurality of transmitters and a plurality of receivers to a transmitter/receiver antenna, comprising the steps of:

connecting each transmitter to a respective one of the plurality of transmitter ports formed on a single integrated circuit die;

connecting each receiver to a respective one of a plurality of received reports formed on the die;

controlling a selected one of a plurality of switching topologies, each associated with a respective one of the transmitter and receiver ports, to connect a respective selected one of the transmitter and receiver ports to an antenna port formed on the die; and

controlling other ones of the switching topologies to isolate others of the transmitter and receiver ports from the antenna port;

for a selected one of the receiver or transmitter ports, switching a transistor having a signal path between an associated one of the receiver or transmitter ports and the antenna to an ON state to pass a signal from said associated receiver or transmitter port through said current path of the signal path transistor;

turning off an associated shunt transistor having a drain connected to a gate of the at least one signal path transistor so as to isolate the gate from ground;

for at least one other receiver or transmitter port, switching a transistor having a signal path between an associated one of the receiver or transmitter ports and the antenna to an OFF state; and

turning on an associated shunt transistor having a drain connected to a gate of the at least one other signal path transistor such that the gate is coupled to ground so as to enhance the isolation of the at least one other receiver or transmitter port from the associated receiver or transmitter port.

22. (Currently Amended) The method of Claim ~~17~~ 21, and further including the steps of:

arranging at least some of the switching topologies in cascaded stages including a first stage coupled to the antenna port and a last stage coupled to a plurality of the transmitter or receiver ports;

connecting a selected one of the last said transmitter or receiver ports to the antenna ports by switching on the first stage, and switching on a switch associated with said selected one of the last said transmitter or receiver ports wherein the last said switch is a portion of the last stage; and

switching off the remaining switching topologies and other switches in the last stage.

23. (Currently Amended) The method of Claim ~~18~~ 22, wherein said step of controlling a selected one of the switching topologies includes the step of switching a plurality of series-connected switching transistors to an ON state.

24. (Cancelled).

25. (New) The integrated circuit of Claim 1 wherein the plurality of FETs further comprises a last one of the FETs proximate the transmission node and having a current path with a first and coupled to the transmission node, the integrated circuit further comprising a second feed-forward capacitor coupled from gate to the first end of said current path of said last one of the FETs.

26. (New) The integrated circuit of Claim 1, further comprising, in each transmitter switching section, a bypass resistor coupled in parallel with the current paths of the plurality of FETs in series.

27. (New) no The integrated circuit of Claim 25, further comprising, in each transmitter switching section, a bypass resistor coupled in parallel with the current paths of the plurality of FETs in series.

28. (New) A single-die integrated circuit for switching among a plurality of transmission ports and a plurality of received reports, comprising:

a transmitter switching section having a plurality of transmission ports, said transmitter ~~control circuitry~~ switching section operable to switch a selected one of the plurality of transmission ports to a transmission node wherein, for each transmission port, the transmission switching section includes a plurality of FETs having current paths coupled in series with each other and operable to couple the transmission port to the transmission node, wherein a last one of the FETs proximate the transmission node has a current path with a first end coupled to the transmission node and a gate;

a first feed-forward capacitor coupled between said first end of said current path and said gate of said last one of the FETs; and

a receiver switching section having a plurality of received ports, said receiver ~~control circuitry~~ switching section operable to switch a selected one of the plurality of received reports to the transmission node.

29. (New) The integrated circuit of Claim 28, further comprising, in each transmitter switching section, a bypass resistor coupled in parallel with the current paths of the plurality of FETs in series.

30. (New) A single-die integrated circuit for switching among a plurality of transmission ports and a plurality of received reports, comprising:

a transmitter switching section having a plurality of transmission ports, said transmitter switching section operable to switch a selected one of the plurality of transmission ports to a transmission node wherein, for each transmission port, the transmission switching section includes a plurality of FETs having current paths coupled in series with each other and operable to couple the transmission port to the transmission node;

a bypass resistor coupled in parallel with the current paths of the plurality of FETs in series; and

a receiver switching section having a plurality of received ports, said receiver switching section operable to switch a selected one of the plurality of received reports to the transmission node.